# Heterogeneous Integration of Enhancement Mode $In_{0.7}Ga_{0.3}As$ Quantum Well Transistor on Silicon Substrate using Thin ($\leq$ 2 $\mu$m) Composite Buffer Architecture for High-Speed and Low-voltage ( 0.5V) Logic Applications


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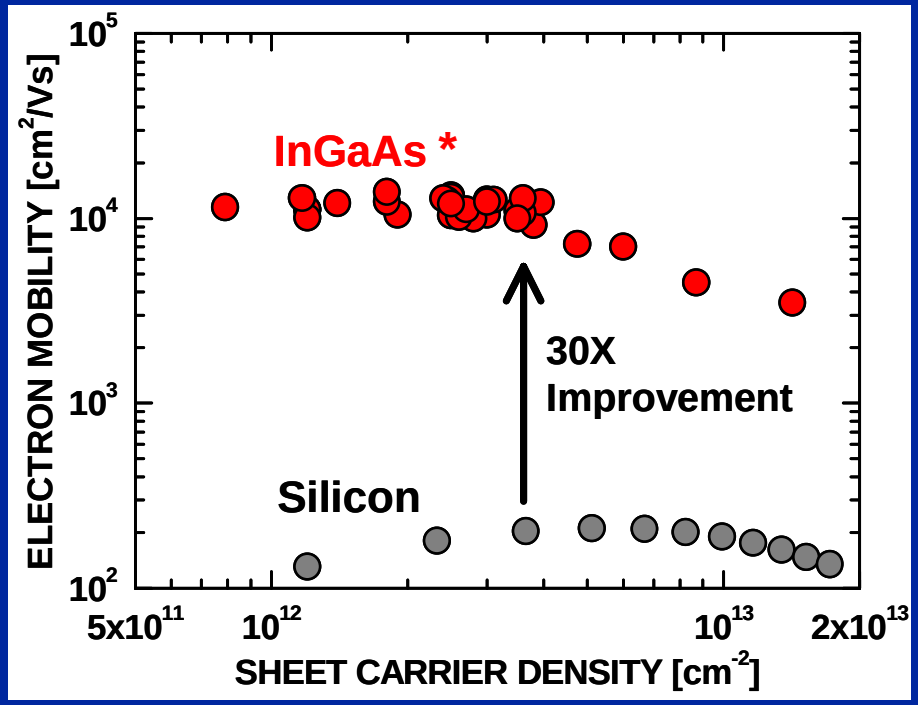
# Outline

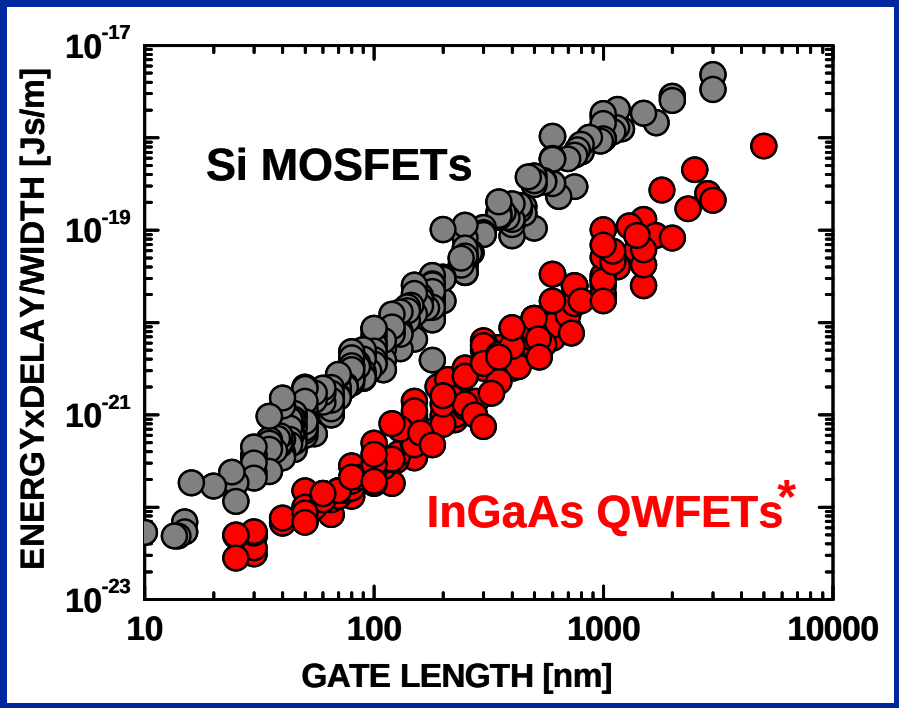
- Motivation
- Materials Integration and Characterization
  - Buffer layer architecture
  - Structural properties
  - Electrical properties
- Transistor Fabrication and Device Results
  - Transistor fabrication process
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  - Benchmarking against Si n-MOSFET
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# Advantages of InGaAs Quantum Well

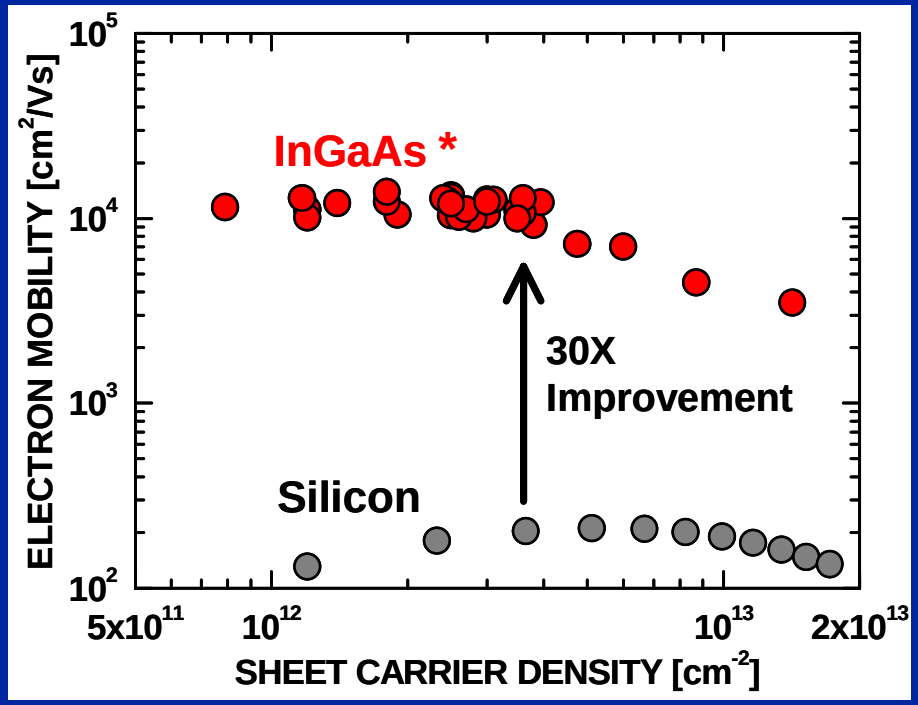


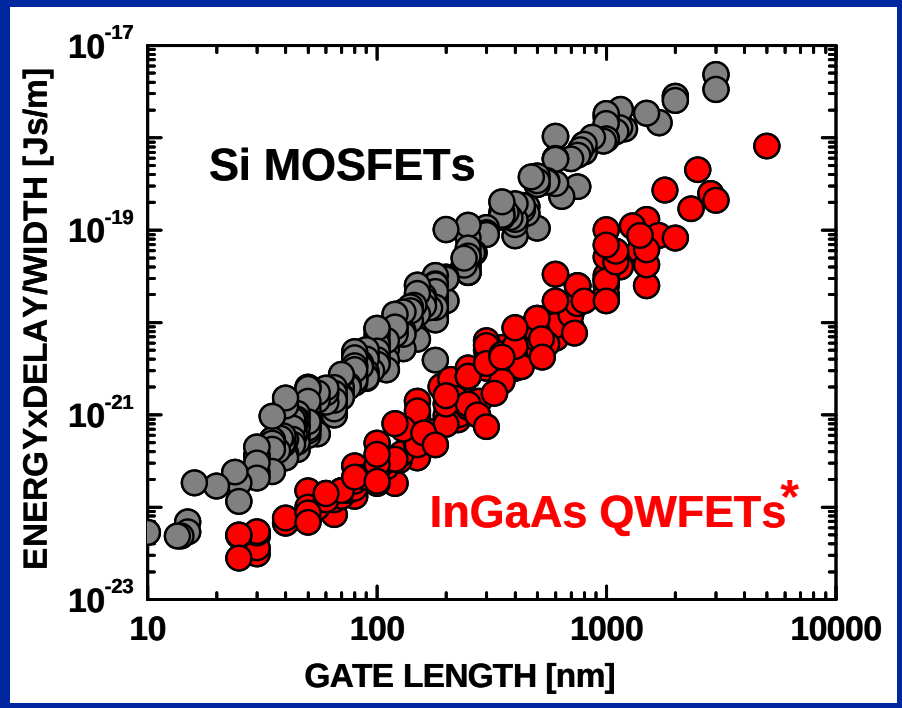




- >30X electron mobility improvement over Si
- lower energy-delay product → better energy efficiency
- potential for low-power and high-speed logic

*R. Chau et al, CSIC (2005), p. 17-20

# Advantages of InGaAs Quantum Well



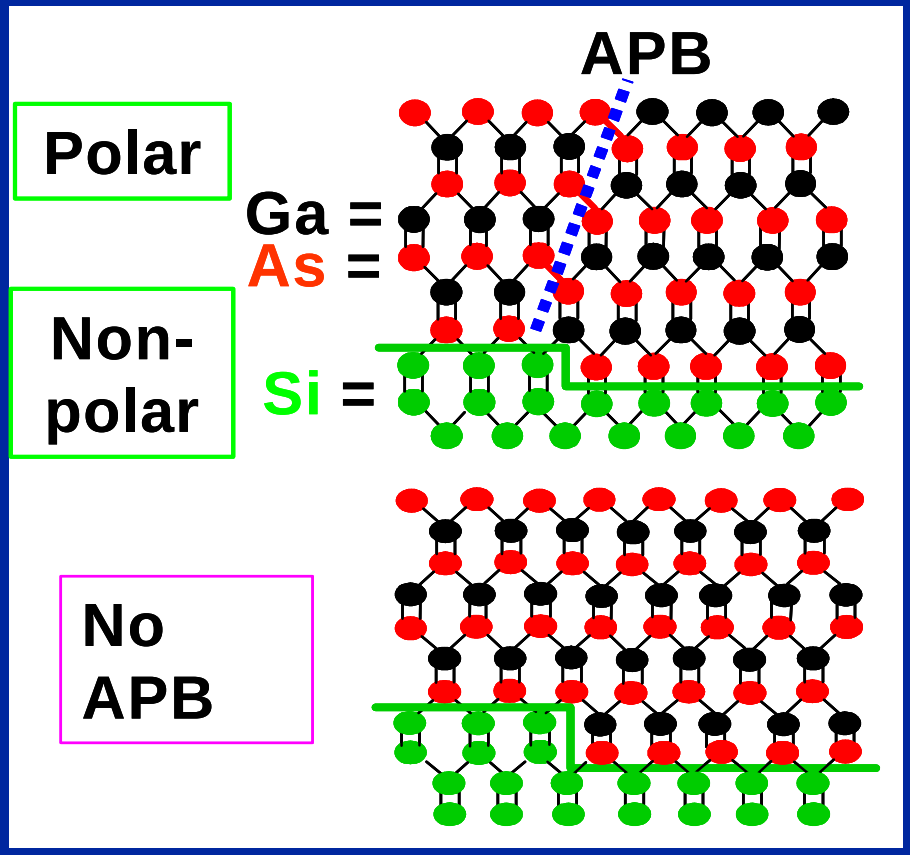



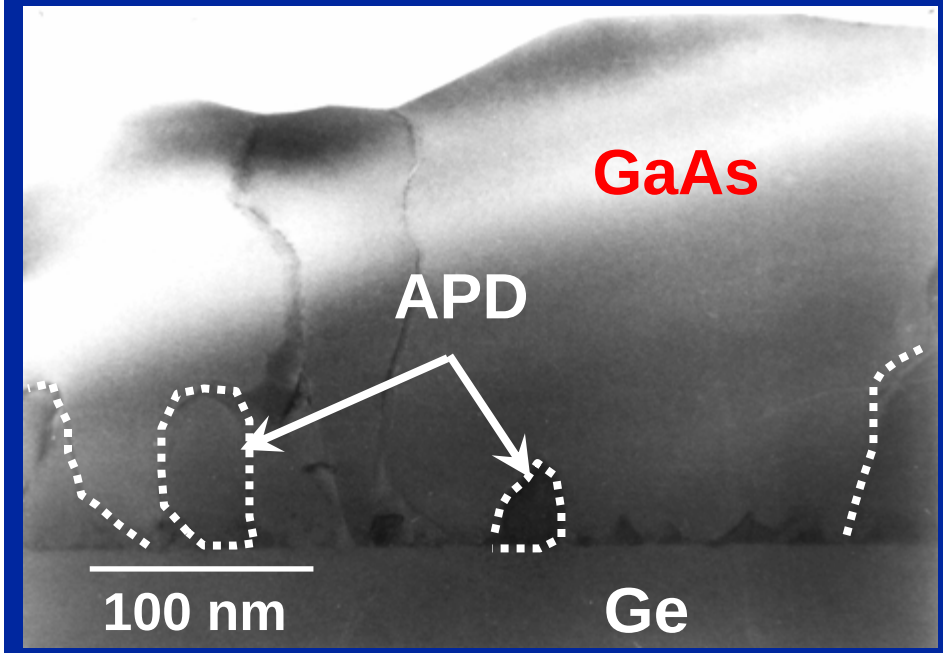

**<u>Question:</u> Can we integrate this high-mobility material onto Si using thin buffer layer without degrading material and transistor properties?**

*R. Chau et al, CSIC (2005), p. 17-20

# Integration Issues of III-V Materials on Si

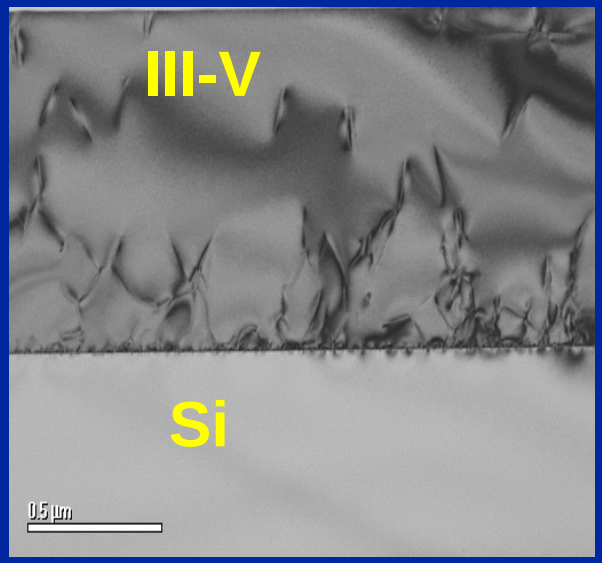
- **Polar/nonpolar interface : Anti-phase domains**



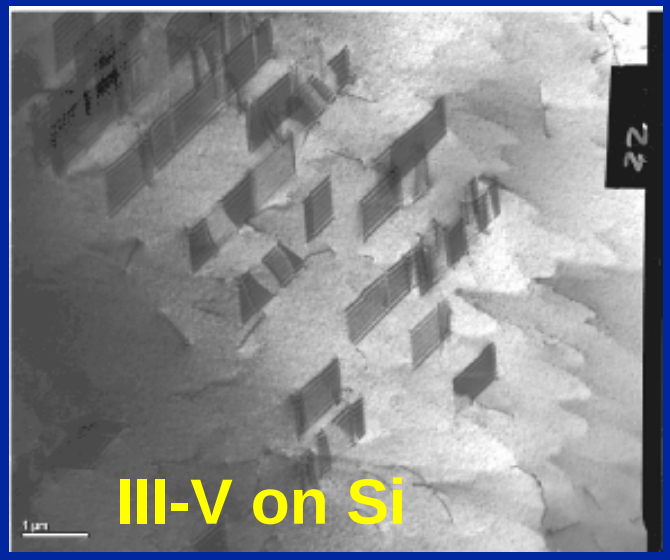



# Integration Issues of III-V Materials on Si

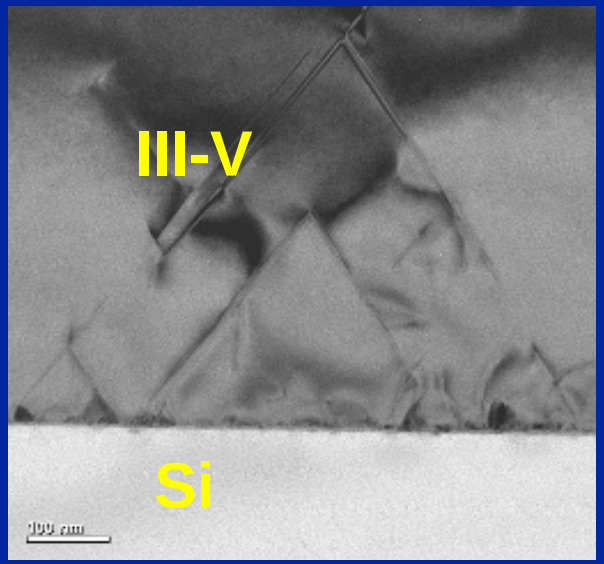
- **Lattice mismatch : Defects and dislocations**




Dislocations



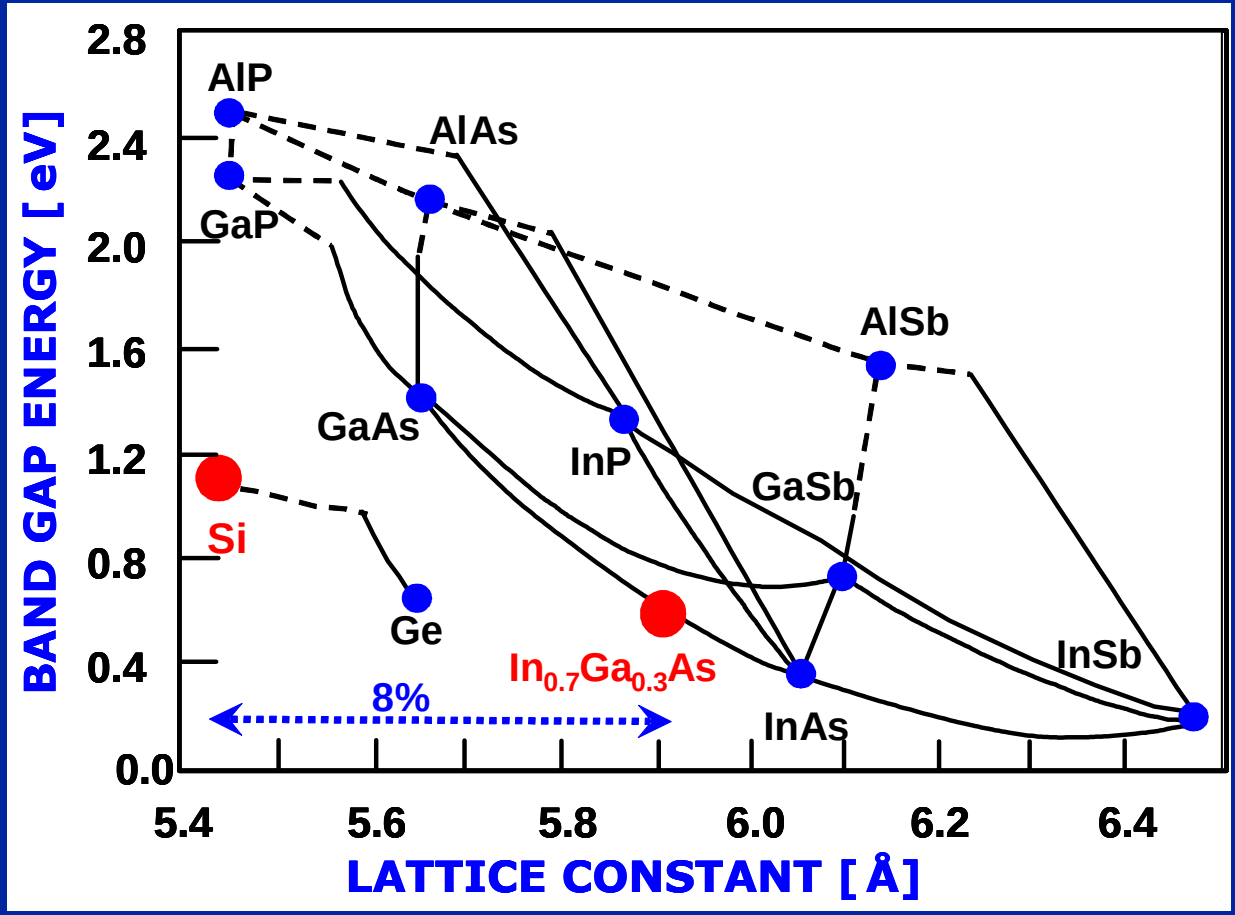

Stacking Faults




Twins

- **Thermal mismatch : Cracks, dislocations, wafer bowing**
- **Chemical mismatch : Interdiffusion, auto-doping**

# Bandgap vs. Lattice Constant of Semiconductors



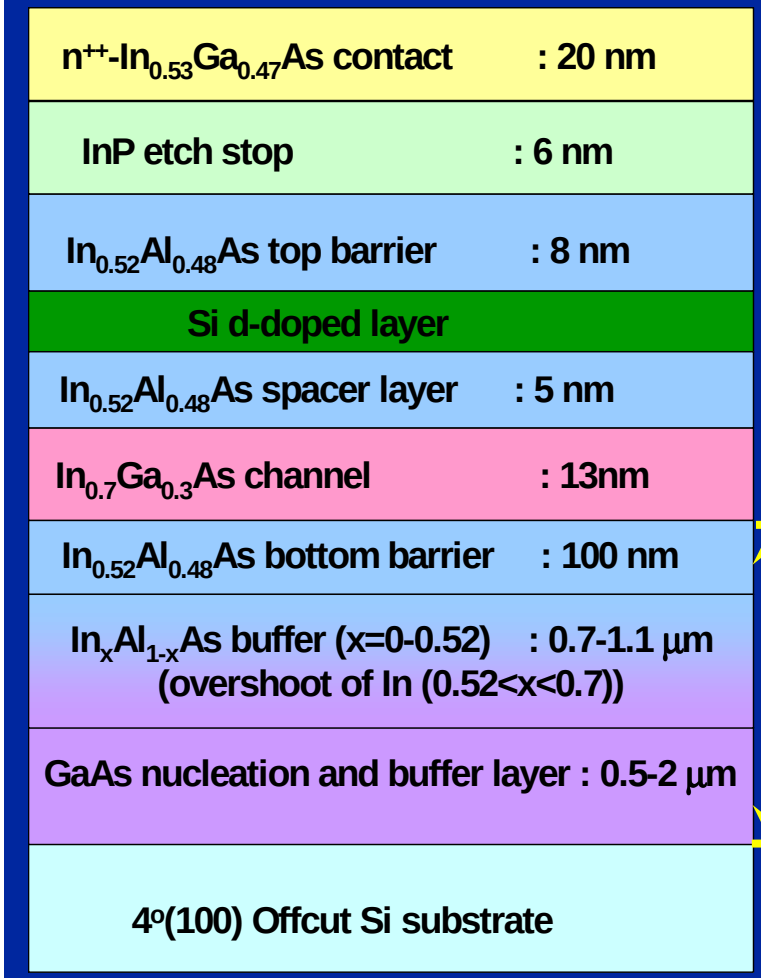

- 8% lattice mismatch between $In_{0.7}Ga_{0.3}As$ and Si

→ needs buffer architecture with large bandgap

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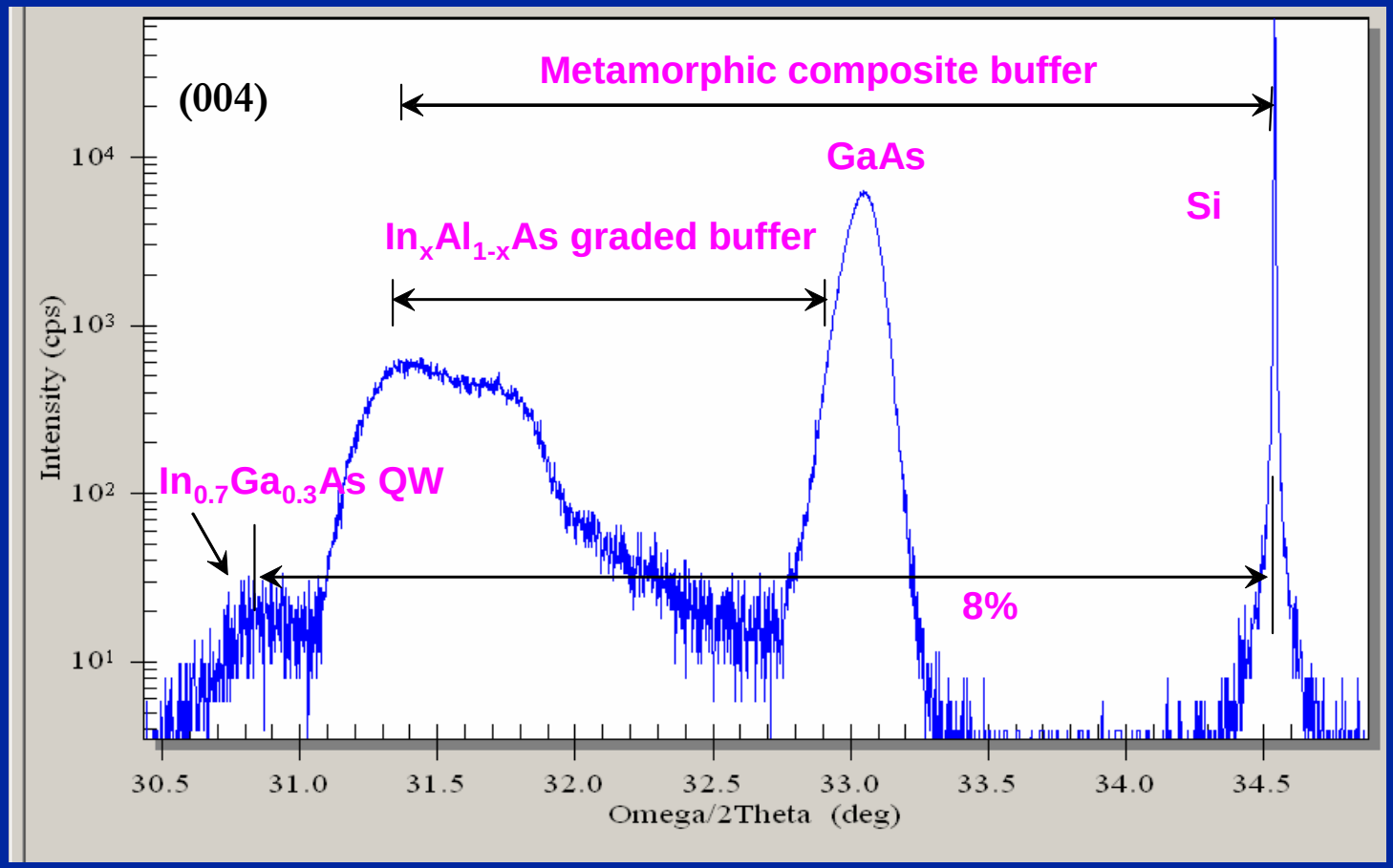
# Buffer Layer Architecture for $In_{0.7}Ga_{0.3}As$ Device Layers on Si




## Metamorphic buffer :

- minimize APDs
- bridge lattice constant
- relax strain energy and glide dislocations
- eliminate parallel conduction
- provide large $\Delta Ec$
- provide strain to QW

# X-ray Rocking Curve of $In_{0.7}Ga_{0.3}As$ QW Device Structure on Si

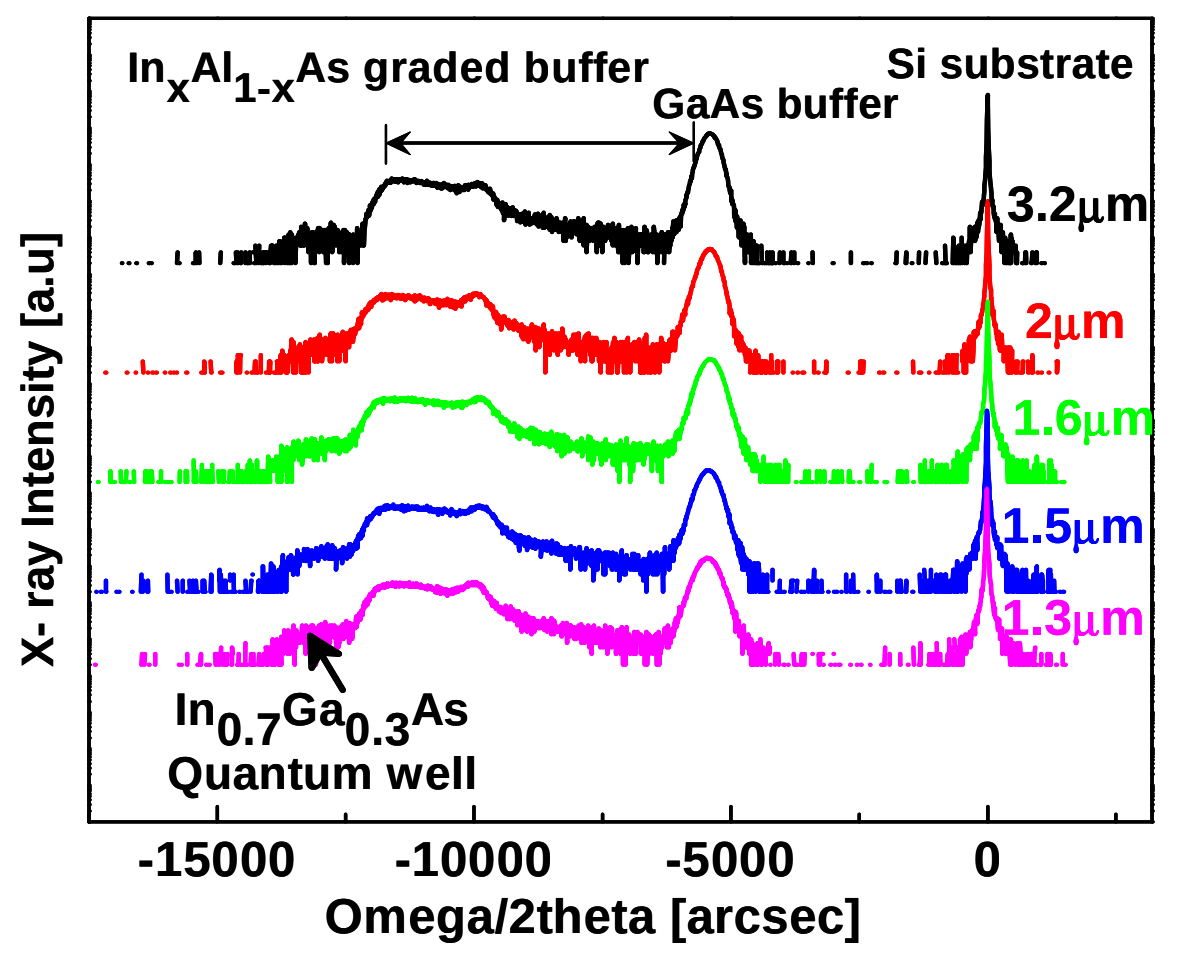



X-ray Intensity (cps)

Omega/2Theta (deg)

- XRD validates presence of buffer layers and grading scheme

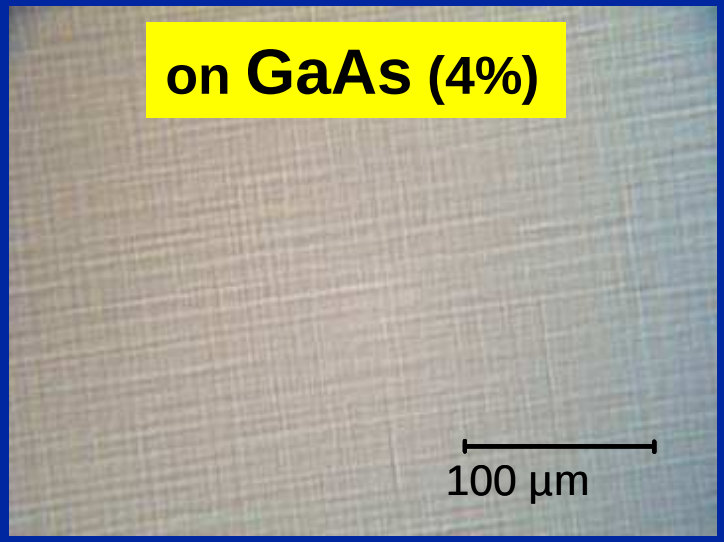
# X-ray Rocking Curves of $In_{0.7}Ga_{0.3}As$ QW Device Structures on Si

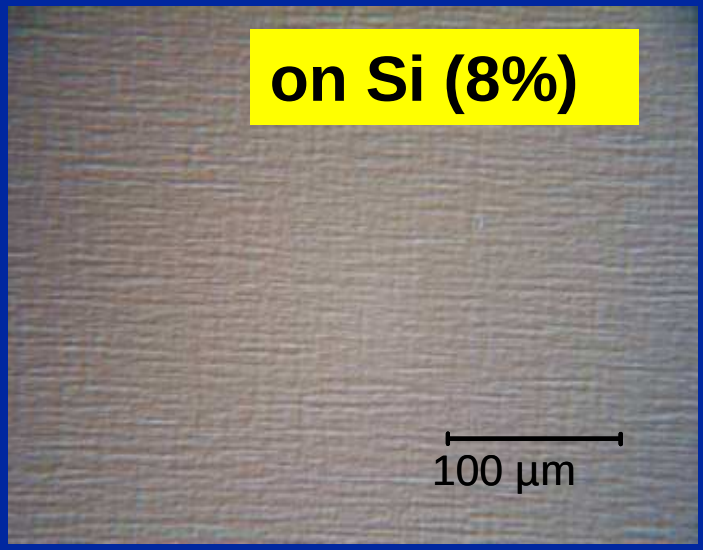



➢Equivalent structural properties with buffer layer thinning

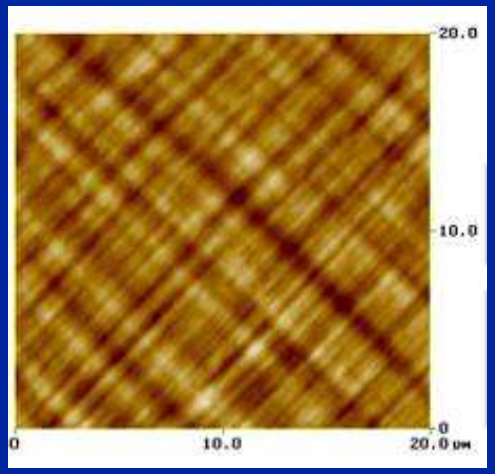
# Surface Morphology of $In_{0.7}Ga_{0.3}As$ QWs

Nomarski



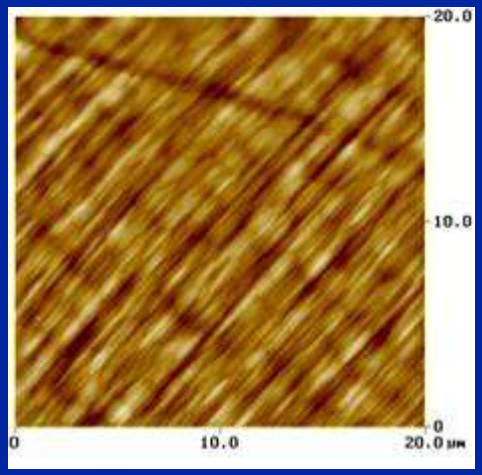




AFM




20µm

20µm

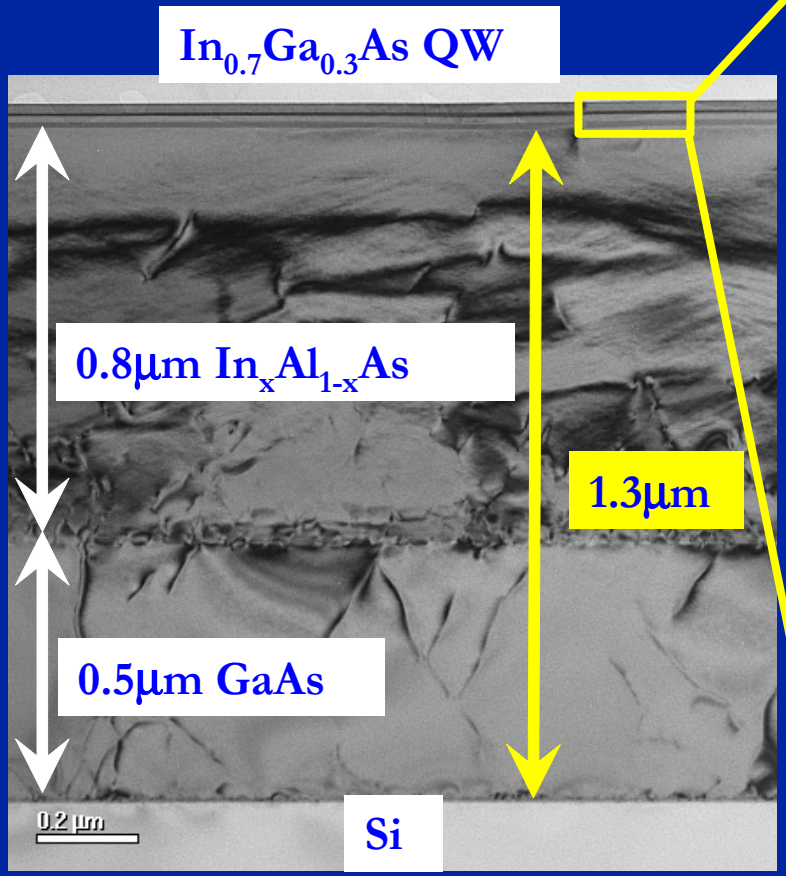


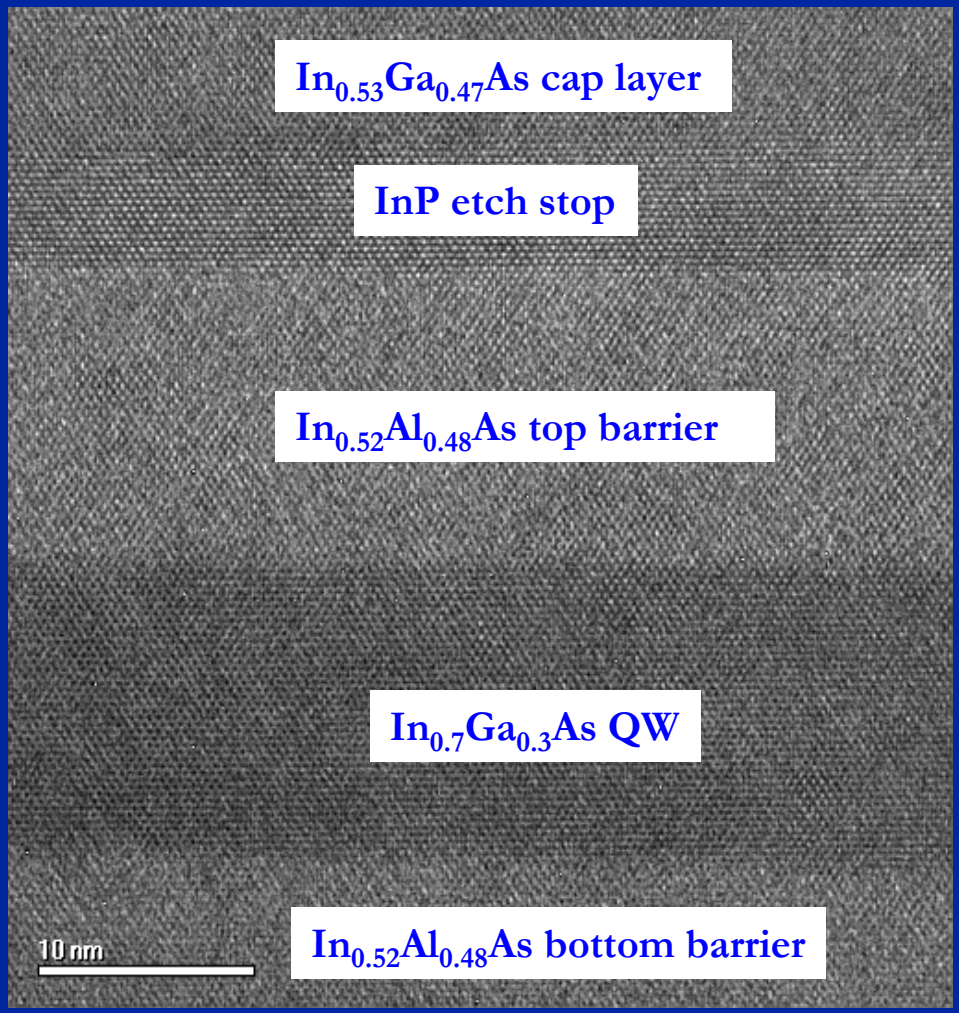

20µm

20µm

➢Cross-hatch morphology indicates good metamorphic buffer layer growth and surface rms roughness <4nm

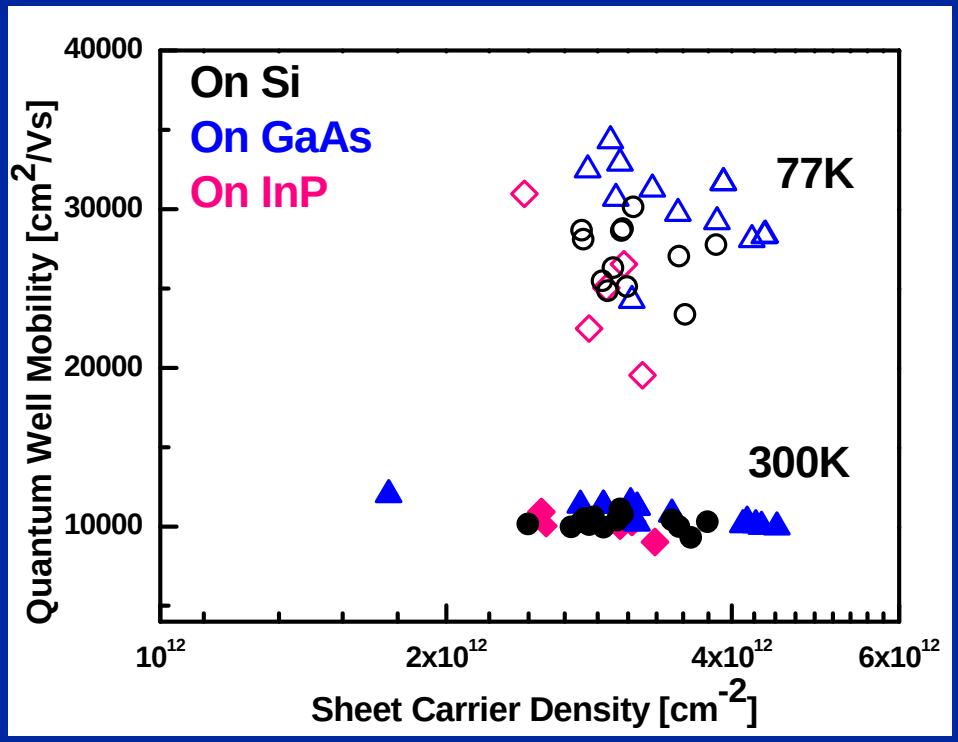
# XTEM Micrographs of $In_{0.7}Ga_{0.3}As$ QW Stack on Si

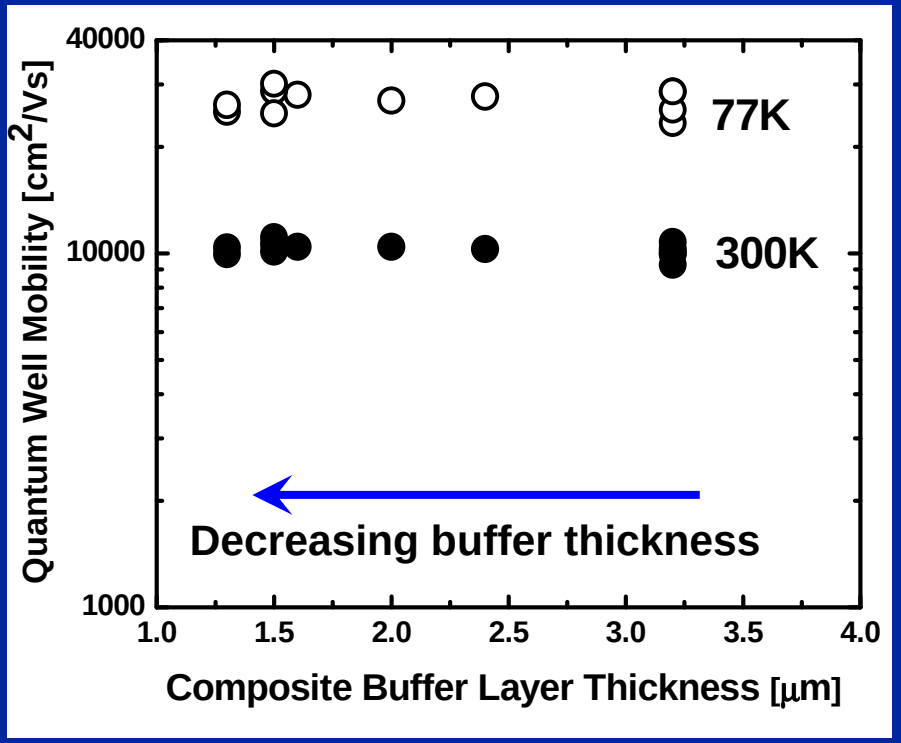



- $In_{0.7}Ga_{0.3}As$ QW stack is virtually defect-free

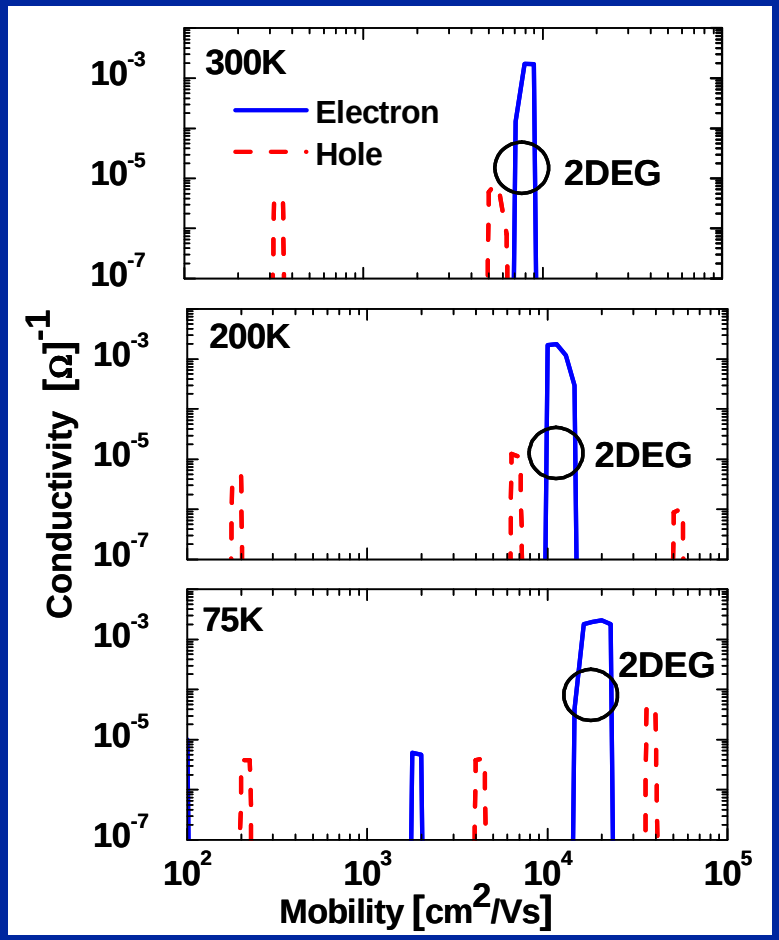
# Carrier Mobility of $In_{0.7}Ga_{0.3}As$ QW on Si

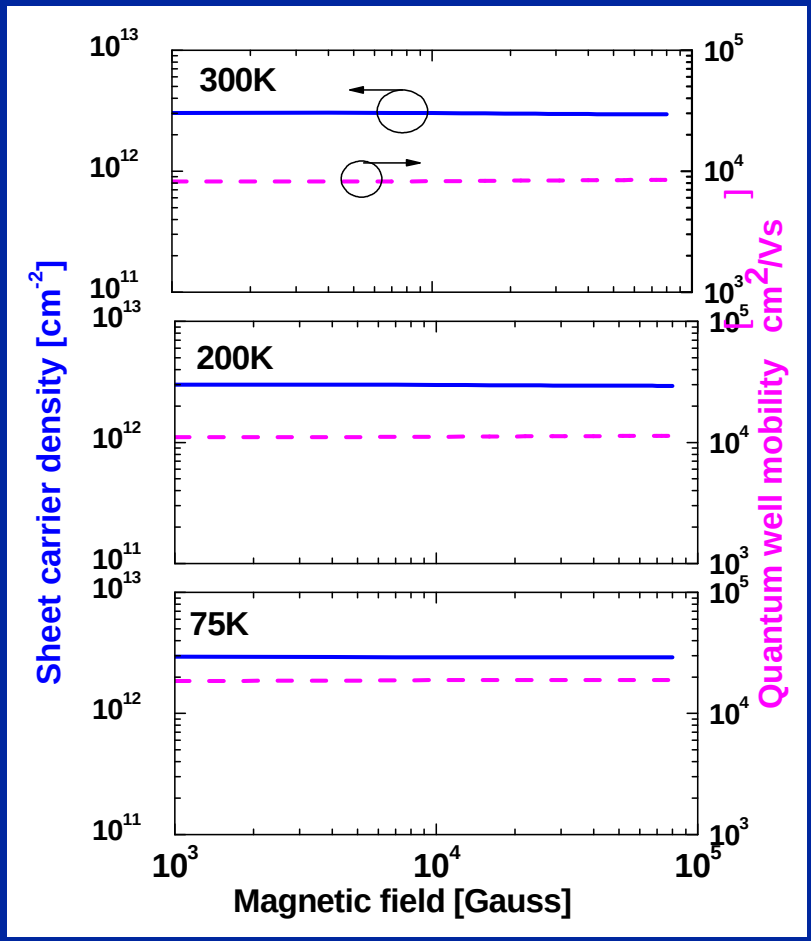



- No QW mobility change regardless of substrate
- No mobility degradation as buffer thickness scaled down to 1.3μm

# Quantitative Mobility Spectrum Analysis of $In_{0.7}Ga_{0.3}As$ QWFET on Si



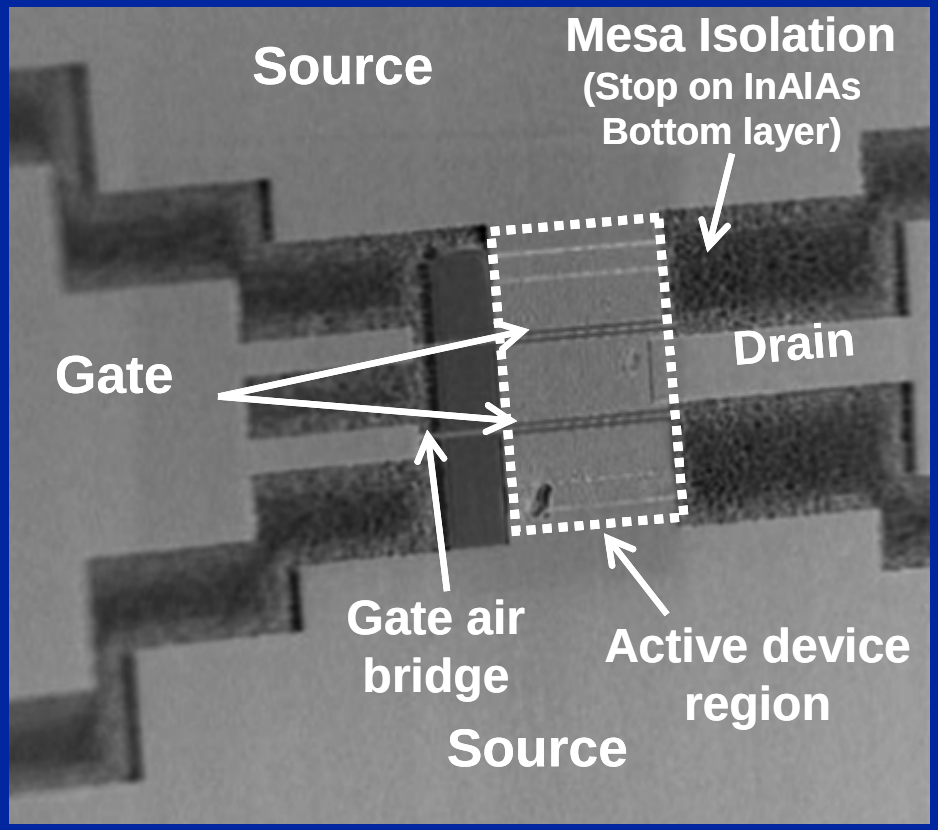



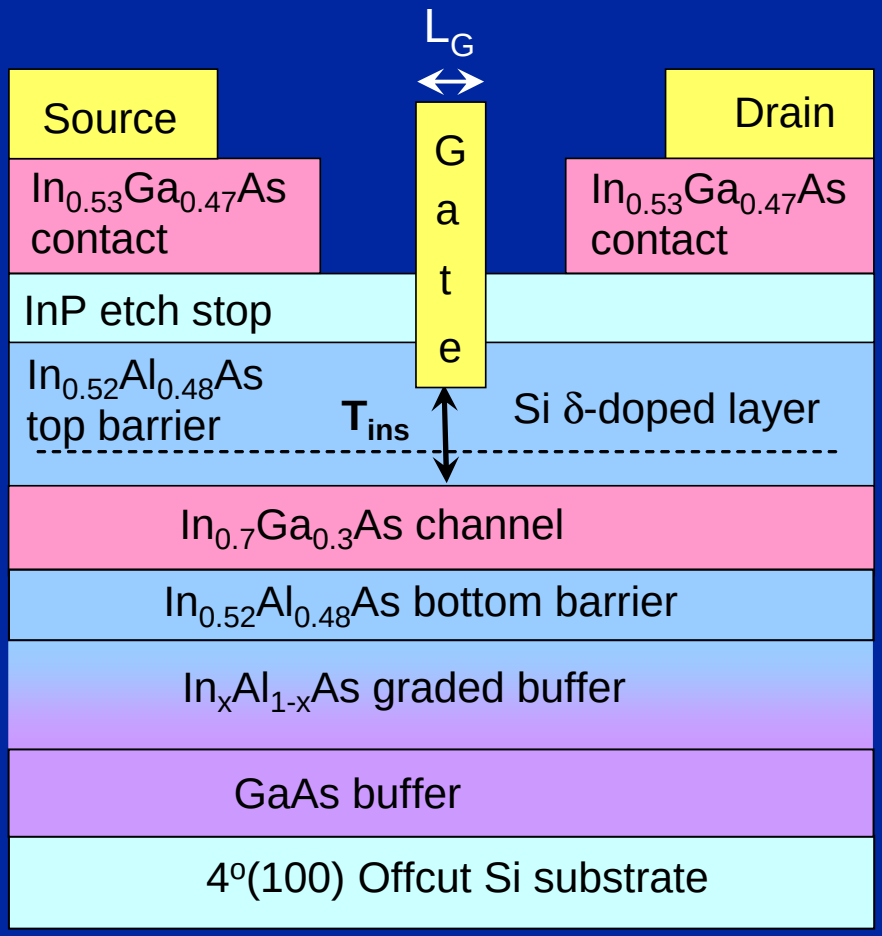

- Higher electron conductivity peak corresponds to QW
- No parasitic channel to $In_{0.7}Ga_{0.3}As$ QW

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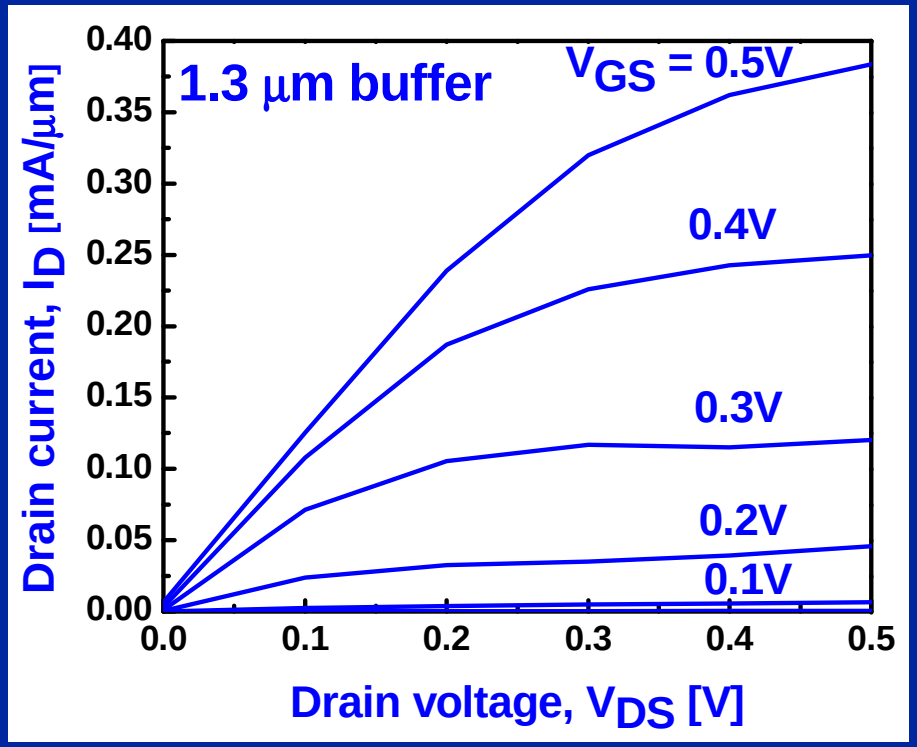
# SEM Micrograph of $In_{0.7}Ga_{0.3}As$ QWFET on Si

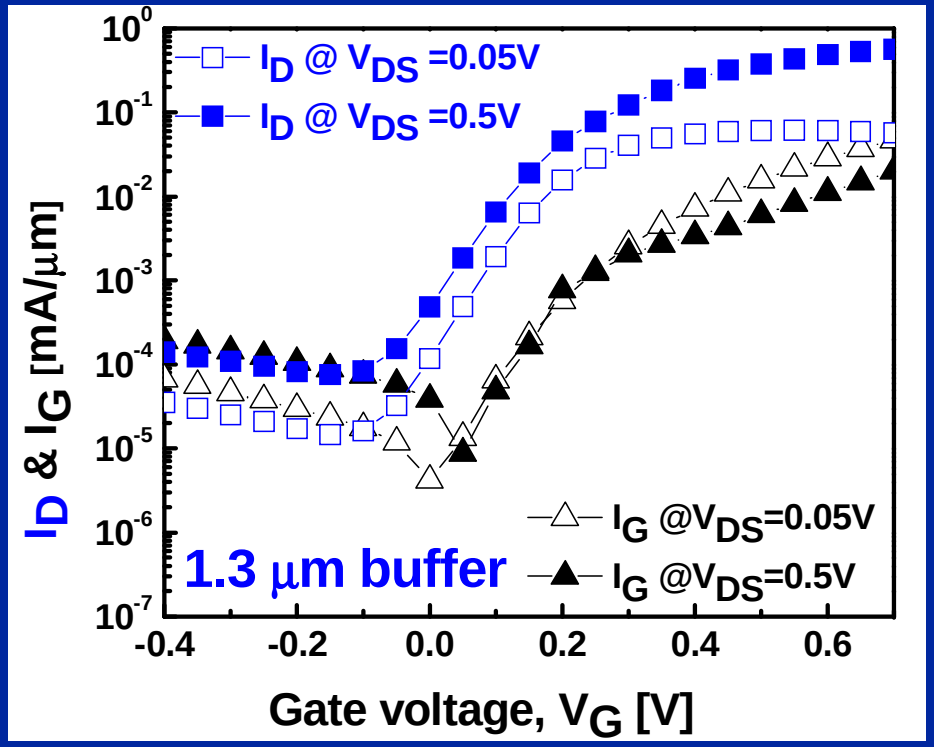



- Pt/Au for gate and Ti/Pt/Au for source/drain contacts

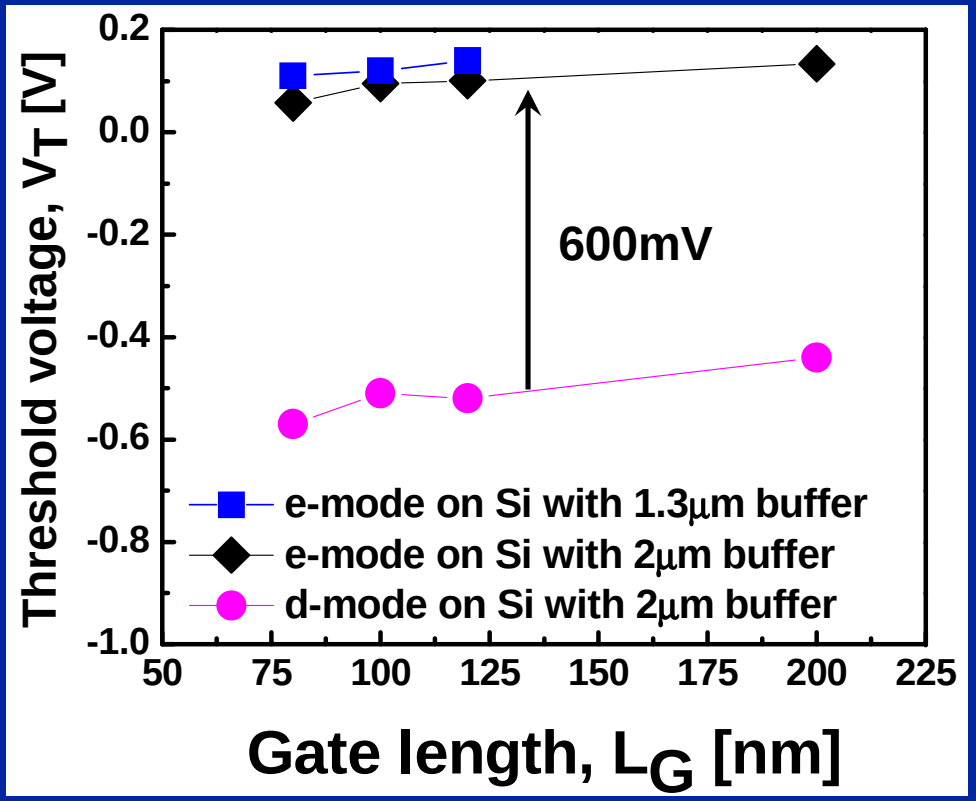
# E-Mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si

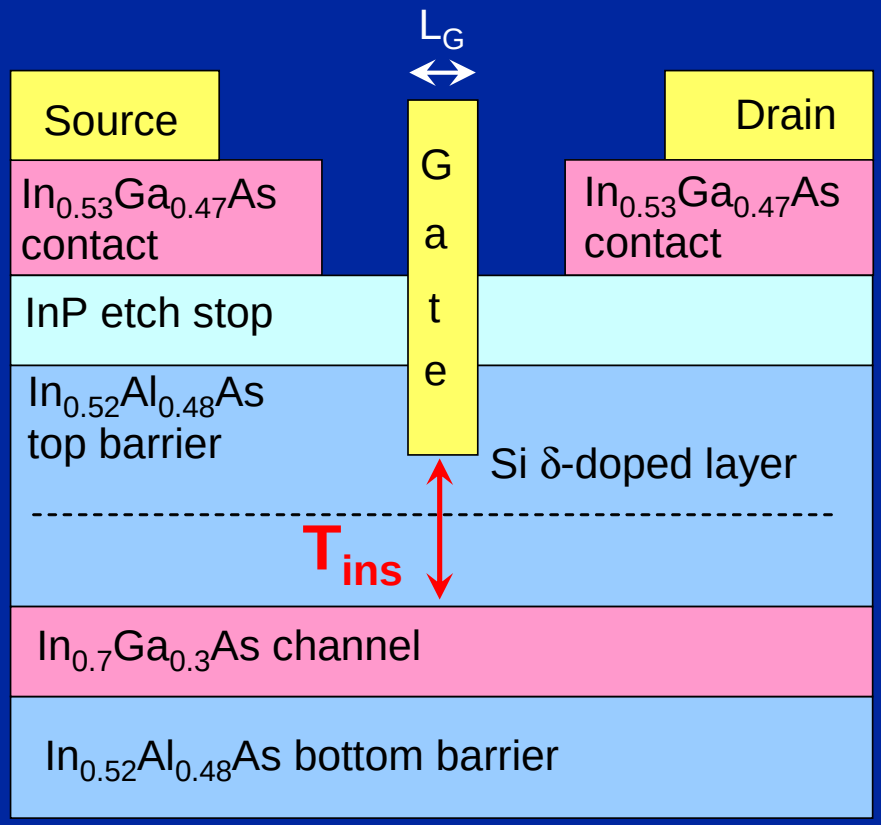



➢Enhancement mode device ($L_G$ = 80nm) with $V_T$ = + 0.11V, $I_{Dsat}$ = 0.32mA/μm and $I_{ON}/I_{OFF}$ = 2150 at $V_{DS}$ = 0.5V with 0.5V $V_G$ swing

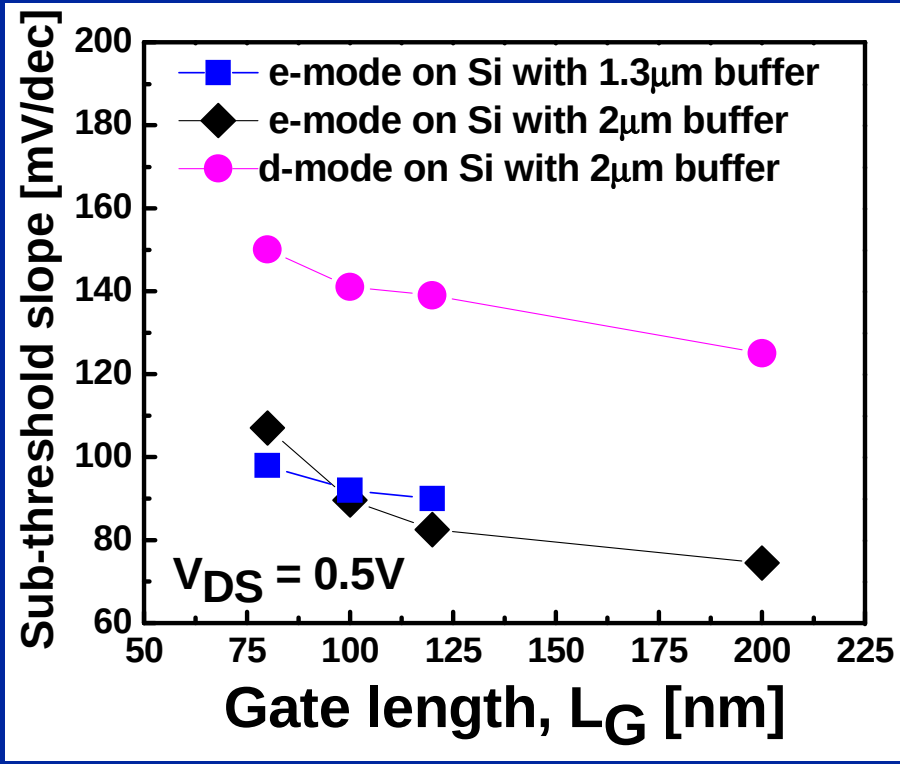
# Depletion-to-Enhancement Mode via $T_{ins}$ Scaling

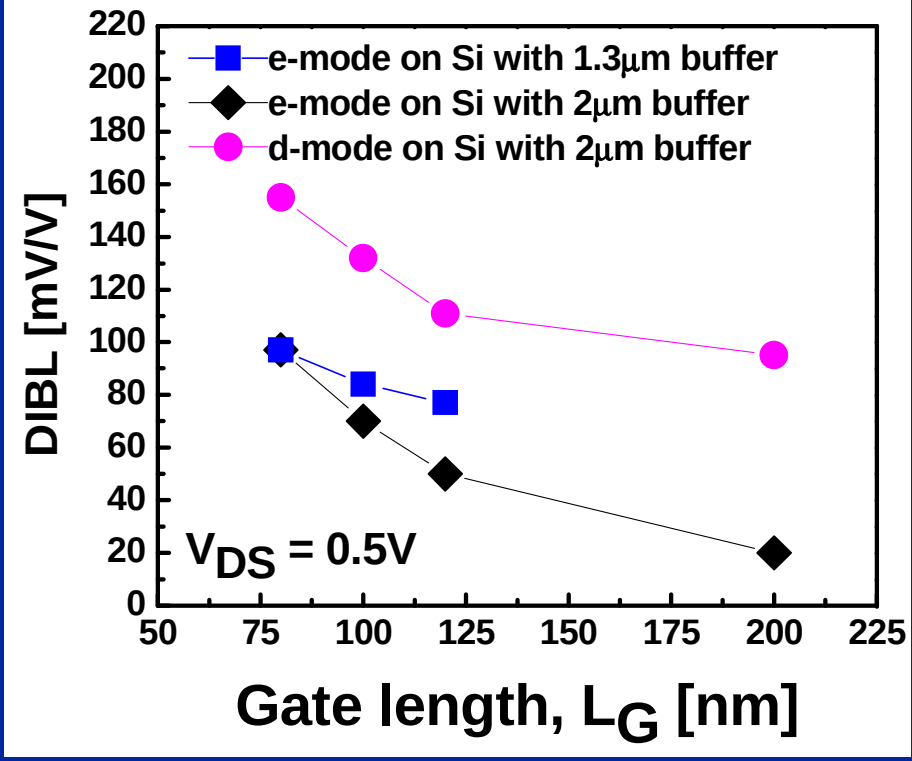



- $T_{ins}$ reduction enables depletion mode to enhancement mode operation

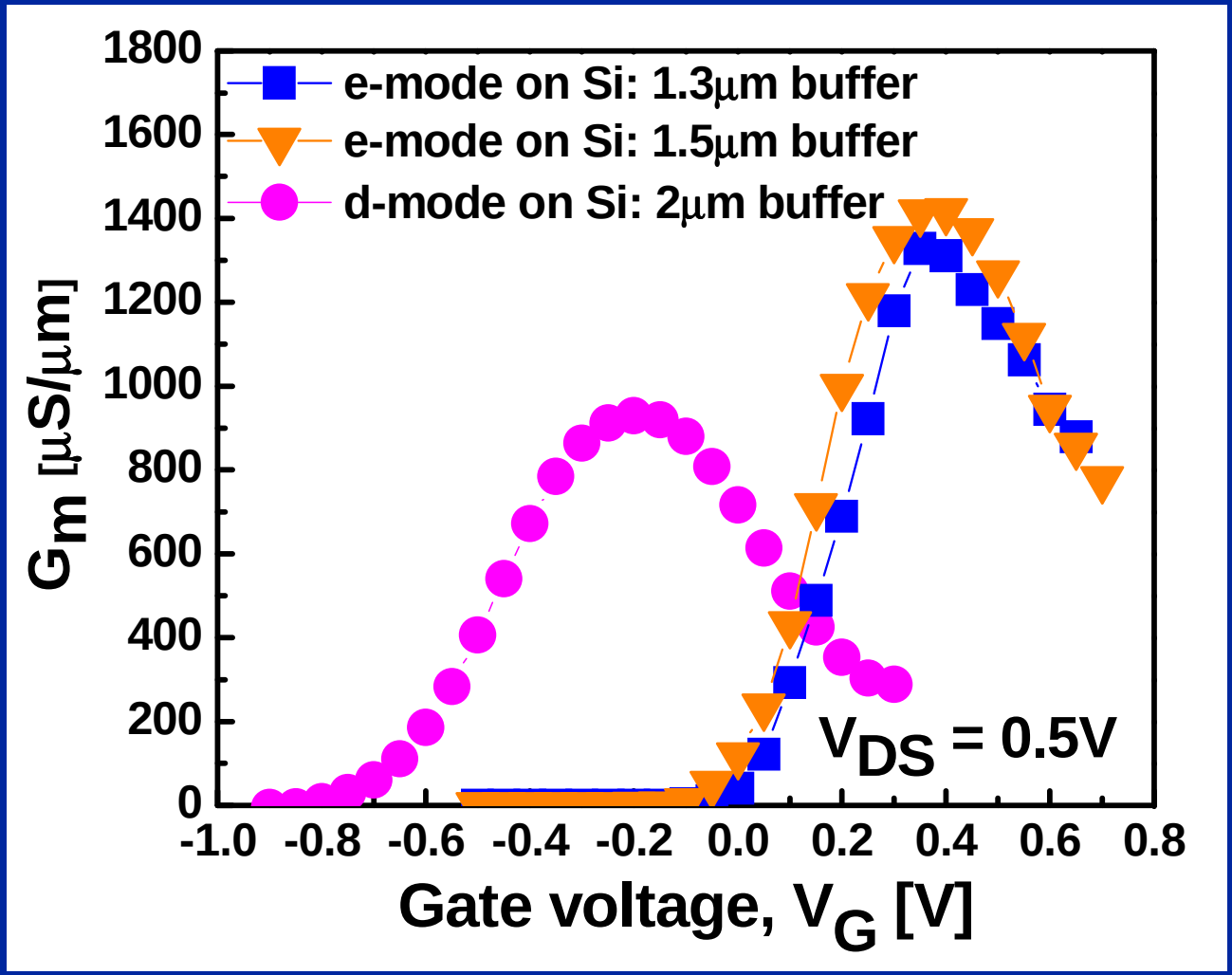
# $T_{ins}$ Reduction Improves Short Channel Effects



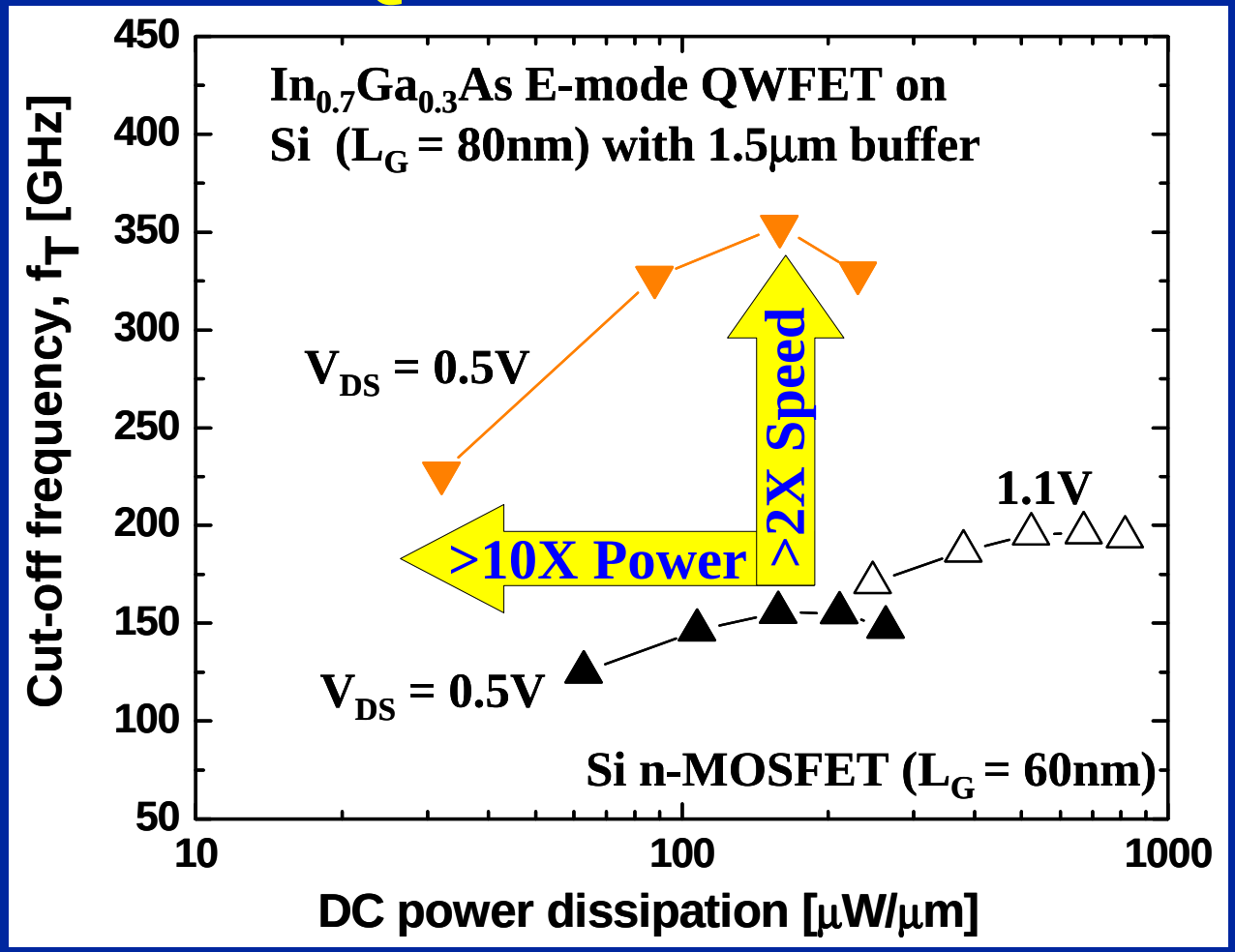

- $T_{ins}$ reduction enables e-mode and improves sub-threshold slope and DIBL

# Transconductance Improvement




- $T_{ins}$ reduction improves transconductance

# Speed-Power Performance of $In_{0.7}Ga_{0.3}As$ QWFET on Si




- $In_{0.7}Ga_{0.3}As$ QWFETs show >10X reduction in power dissipation at same speed compared to Si n-MOSFETs

# Summary

- Heterogeneous integration of high-performance InGaAs QWFETs on Si demonstrated for the first time
- No QW mobility degradation with buffer thickness down to 1.3μm
- No parasitic conduction to $In_{0.7}Ga_{0.3}As$ QW
- Enhancement mode operation achieved through scaling $T_{ins}$ thickness
- InGaAs QWFETs on Si exhibit >10X reduction in power dissipation for the same speed or >2X gain in speed performance for the same power

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